

THE SYMBOL MARK OF THIS SCHEMATIC DIAGRAM INCORPORATES SPECIAL FEATURES IMPORTANT FOR PROTECTION FROM X-RADIATION. FILRE AND ELECTRICAL SHOCK HAZARDS, WHEN SERVICING IF IS ESSENTIAL THAT ONLY MANUFACTURES SPECIFIED PARTS BE USED FOR THE CRITICAL COMPONENTS IN THE SYMBOL MARK OF THE SCHEMATIC.

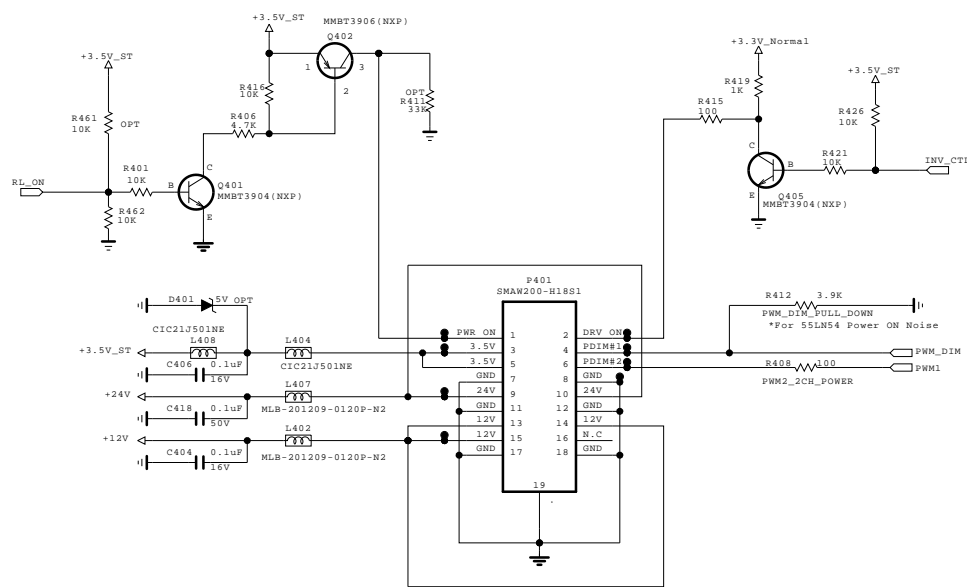
SECRET
LGElectronics



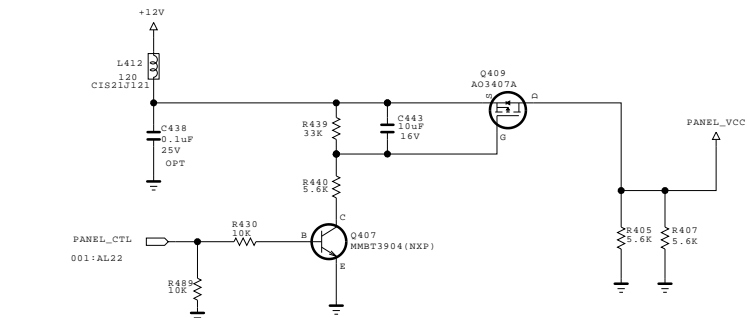
| | | | |
|-------|-------------|-------|------------|
| MODEL | NC4_S7LRM | DATE | 2012/07/05 |
| BLOCK | MAIN1_EU_OS | SHEET | 1 |

L13 POWER BLOCK (POWER DETECT 2)

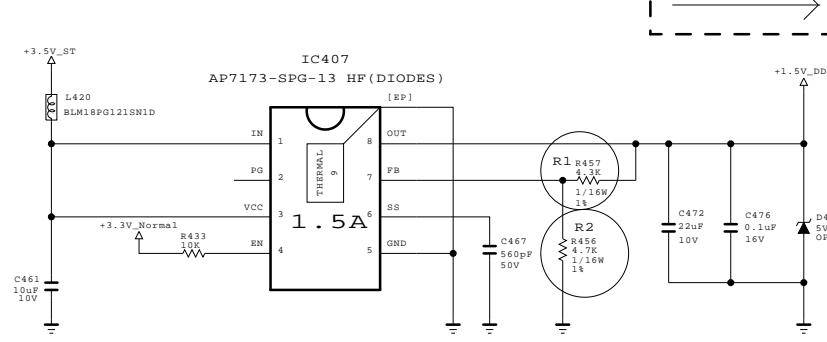
FROM LIPS & POWER B/D



PANEL_POWER

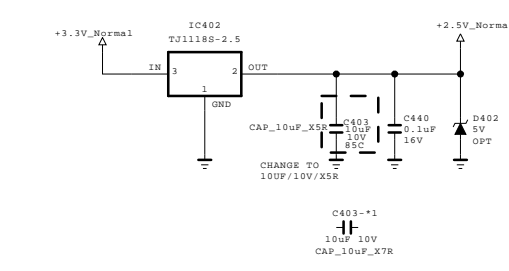


+1.5V_DDR

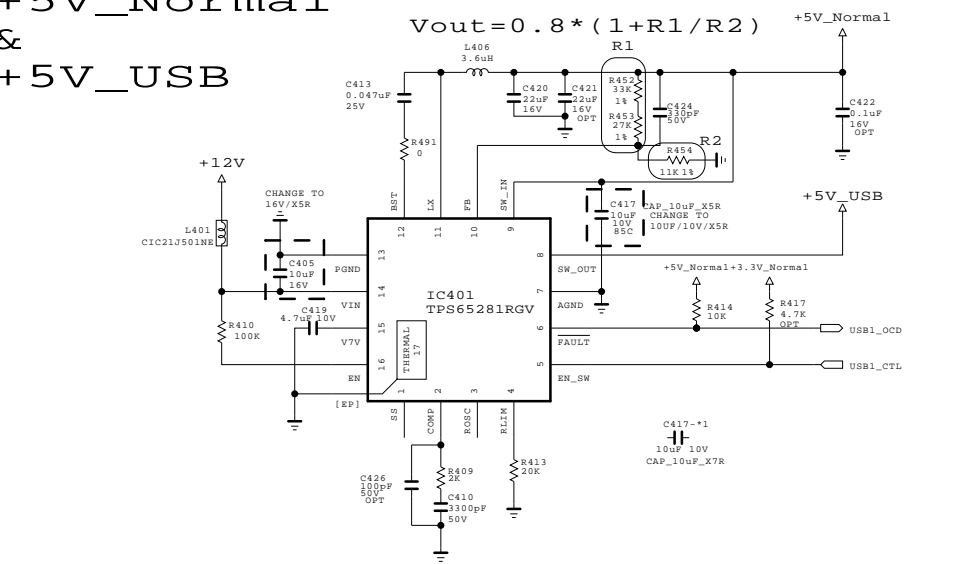


$$V_{out} = 0.8 * (1 + R1/R2) = 1.5319$$

+2.5V_Normal



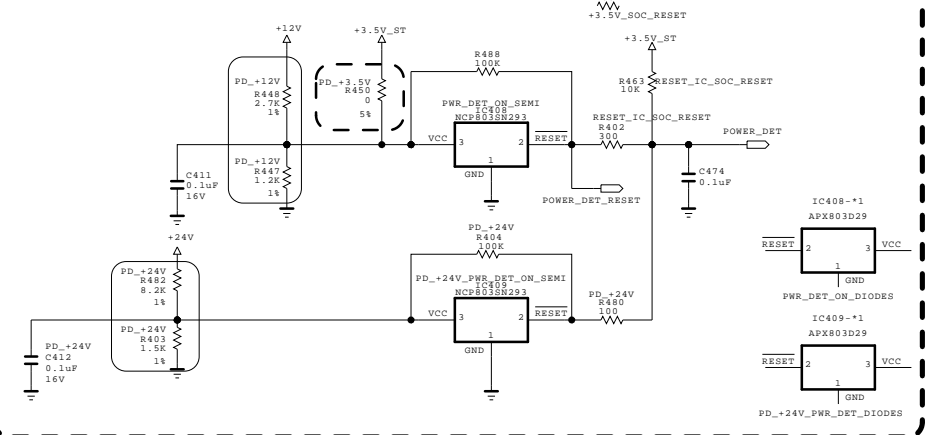
+5V_Normal & +5V_USB



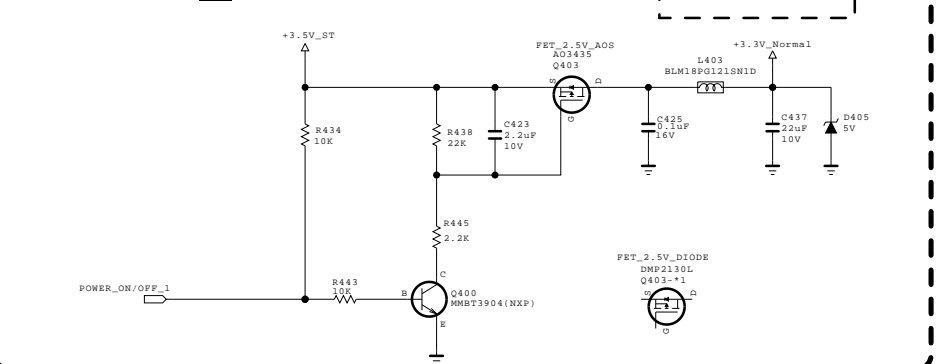
$$V_{out} = 0.8 * (1 + R1/R2)$$

Power_DET

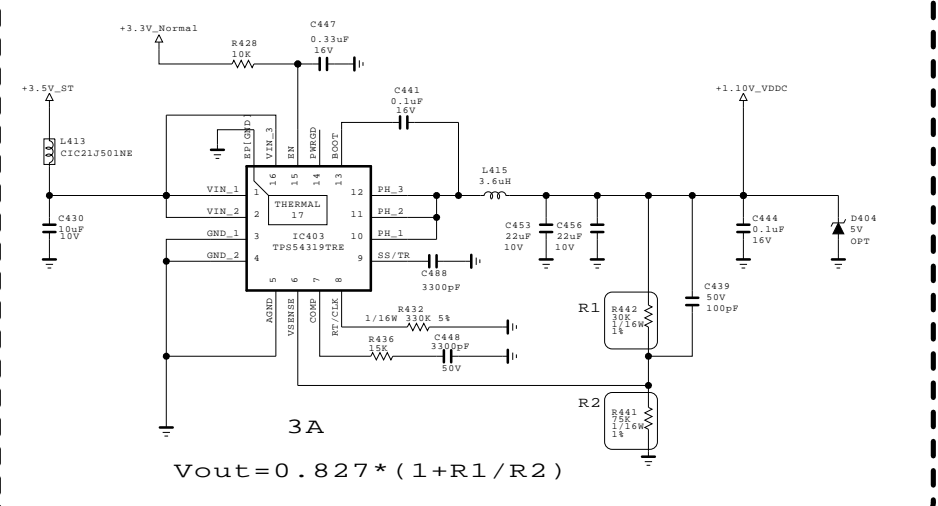
+3.5V_ST --> 3.375V --> 3.46V
 +24V --> 3.78V --> 3.92V (3.79V)
 +12V --> 3.58V --> 3.82V (3.68V)



+3.3V_Normal



S7LR core 1.15V volt



$$V_{out} = 0.827 * (1 + R1/R2)$$

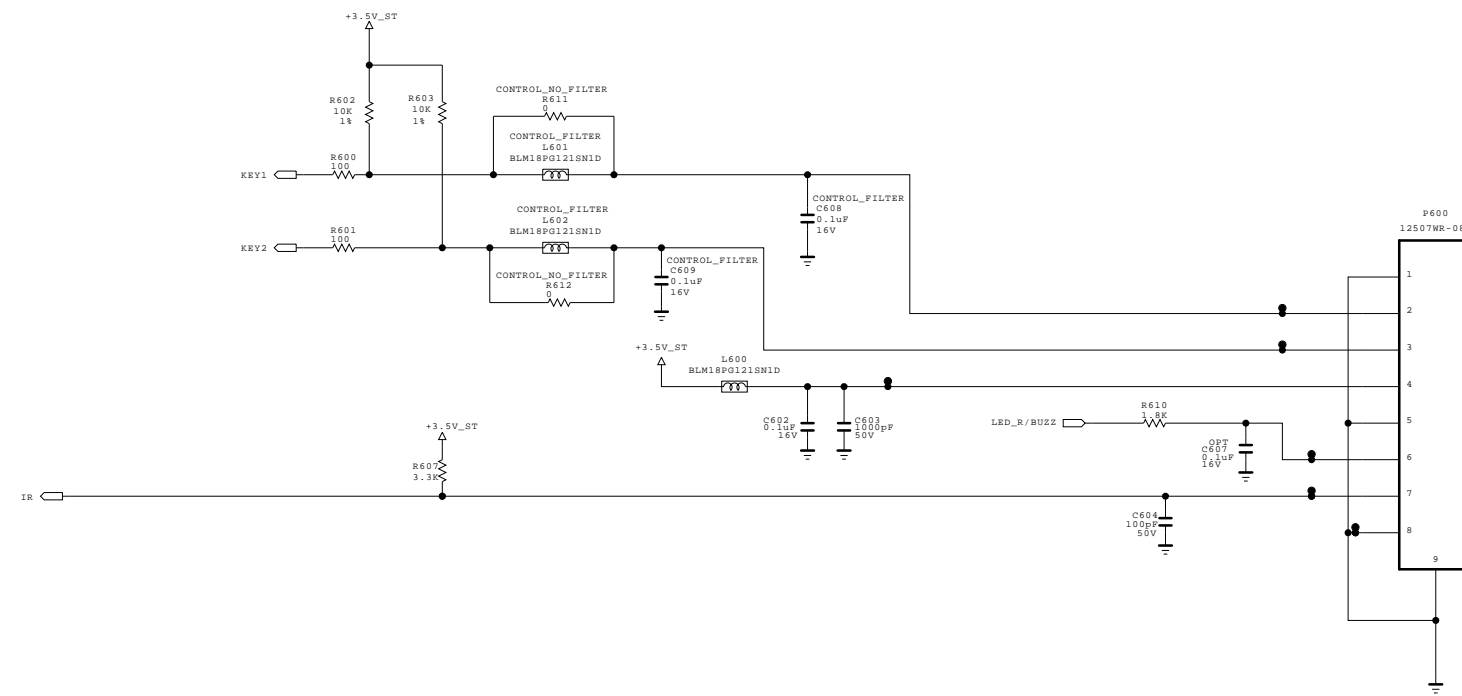
THE Δ SYMBOL MARK OF THIS SCHEMATIC DIAGRAM INCORPORATES SPECIAL FEATURES IMPORTANT FOR PROTECTION FROM X-RADIATION. FILRE AND ELECTRICAL SHOCK HAZARDS, WHEN SERVICING IF IS ESSENTIAL THAT ONLY MANUFACTURES SPECIFIED PARTS BE USED FOR THE CRITICAL COMPONENTS IN THE Δ SYMBOL MARK OF THE SCHEMATIC.



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 LG Electronics



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| MODEL | NC4_S7LRM | DATE | 2012/09/19 |
| BLOCK | Power_PD2 | SHEET | 4 |

IR/LED and Control



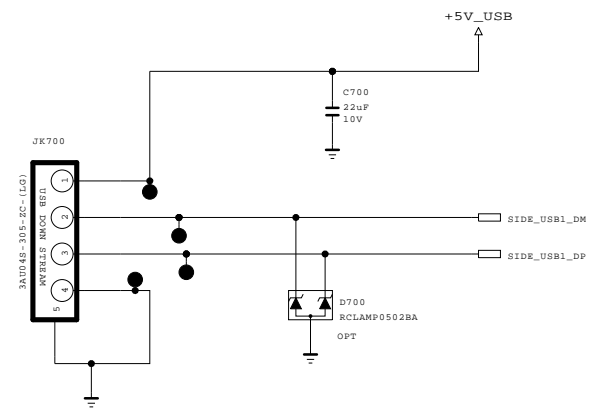
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
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|-------|------------|-------|------------|
| MODEL | NC4_S7LRM | DATE | 2012/07/18 |
| BLOCK | IR/CONTROL | SHEET | 6 / |

USB (SIDE)



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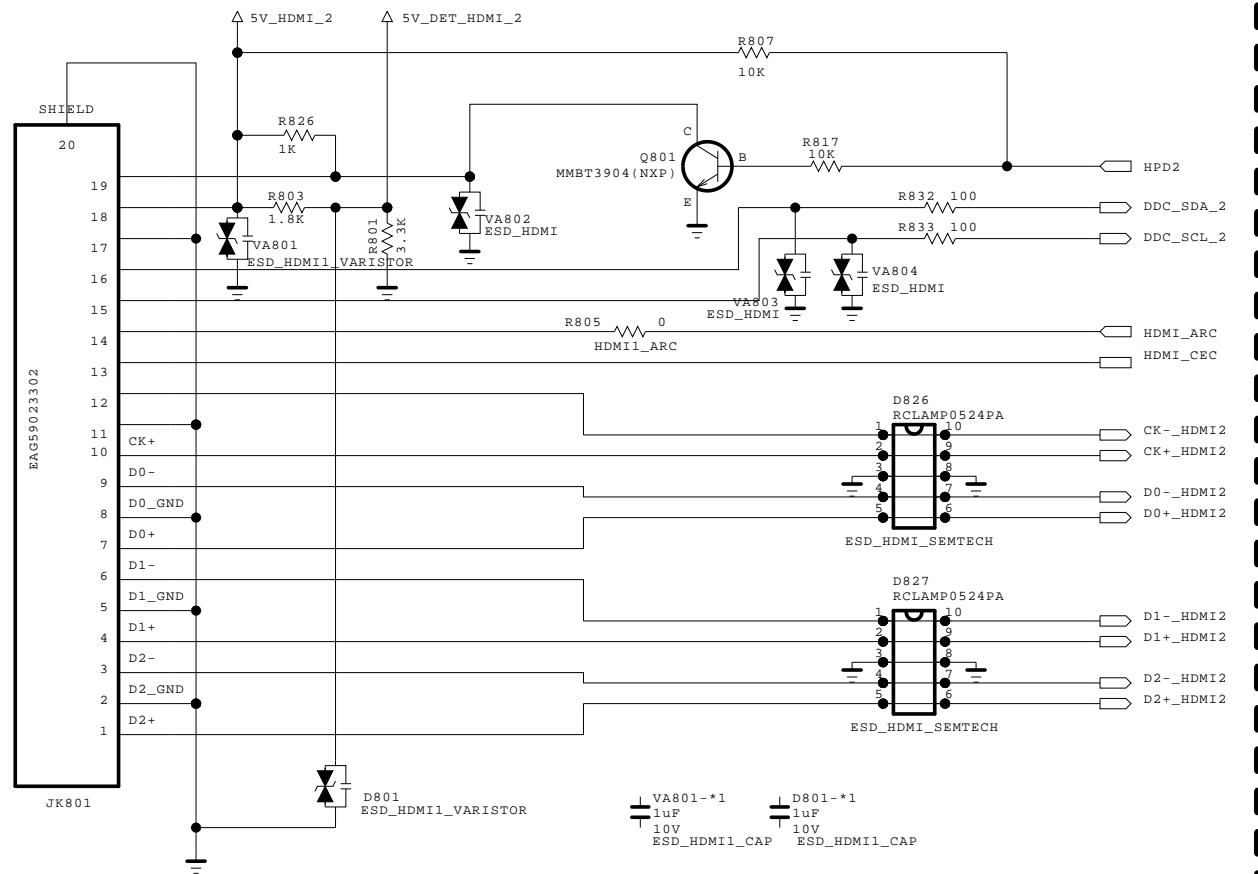
SECRET
LGElectronics



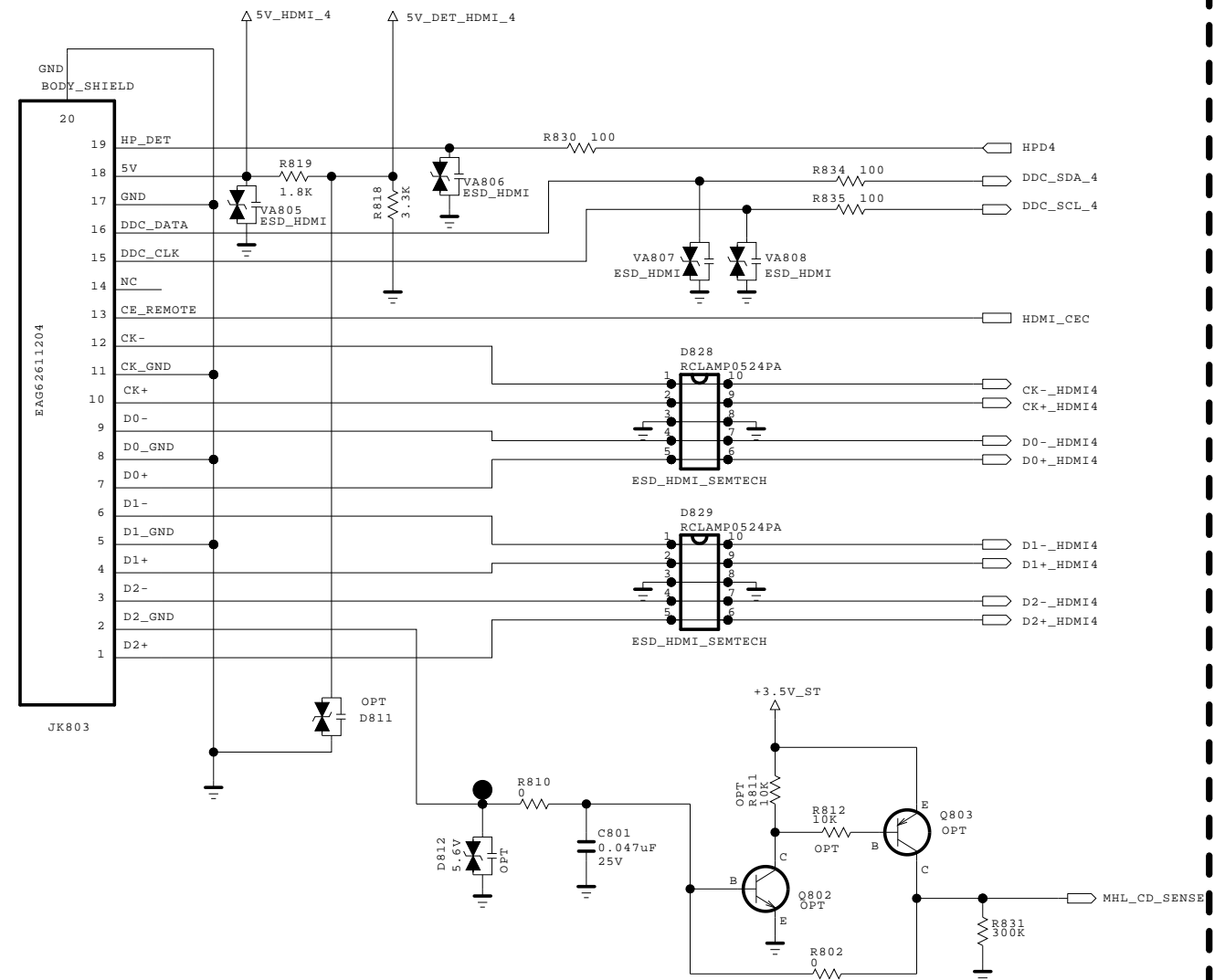
| | | | |
|-------|-----------|-------|----------|
| MODEL | NC4_S7LRM | DATE | 12/06/20 |
| BLOCK | USB | SHEET | 7 / |

HDMI (REAR 1 / SIDE 1 MHL)

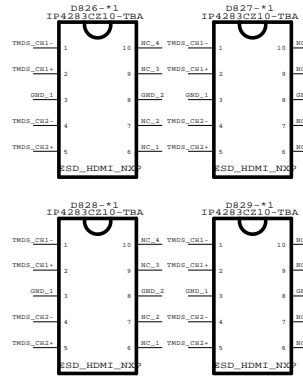
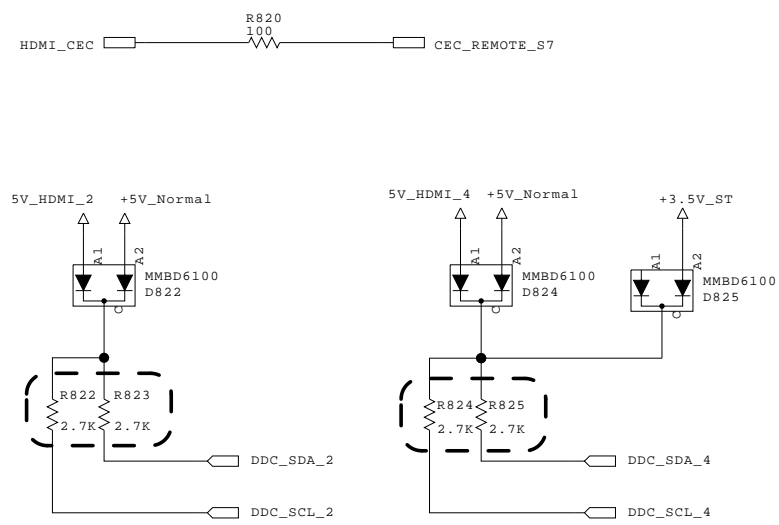
HDMI_1



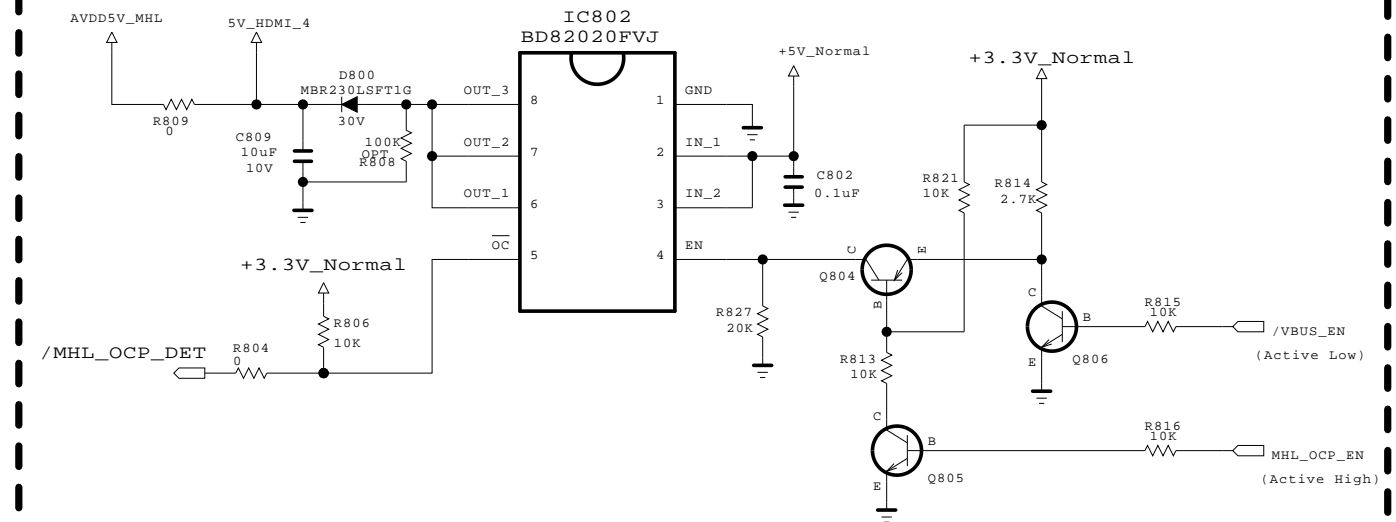
SIDE_HDMI (MHL)



CEC



MHL OCP

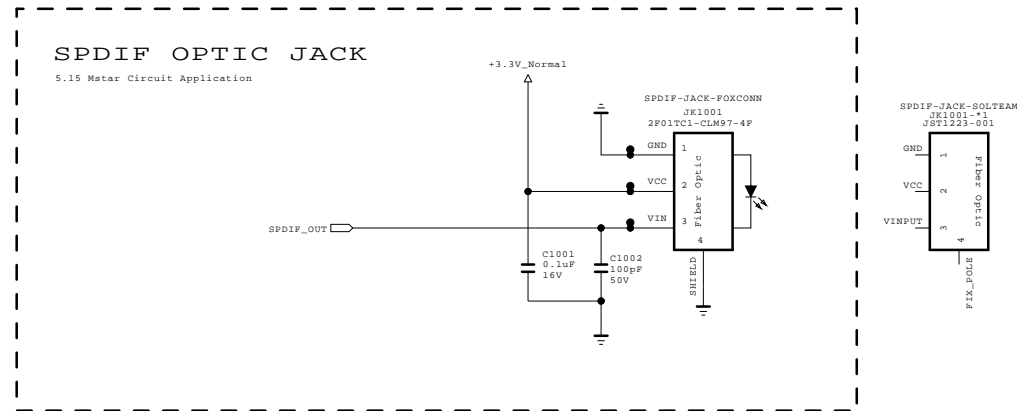


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| MODEL | NC4_S7LRM | DATE | 2012/07/12 |
| BLOCK | HDMI_R1_S1 | SHEET | 8 / |

SPDIF



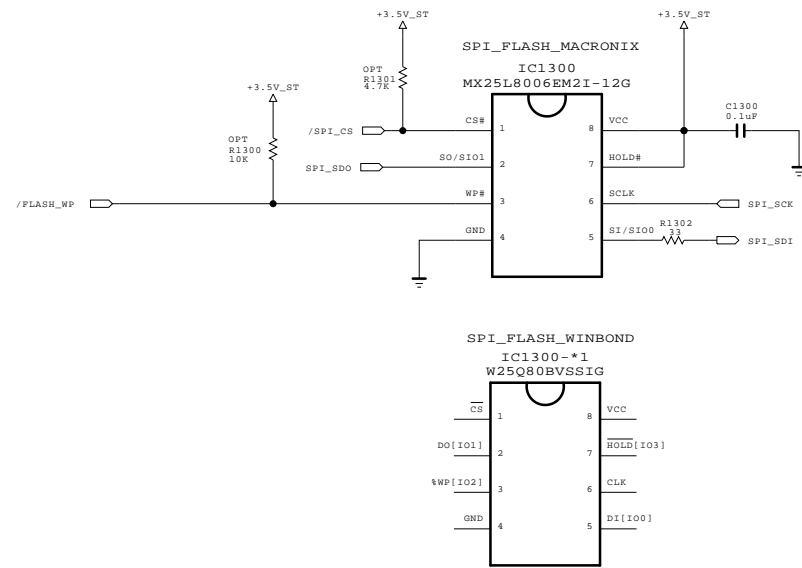
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

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| MODEL | NC4_S7LRM | DATE | 12/06/12 |
| BLOCK | SPDIF | SHEET | 10 / |

Serial Flash for SPI boot(OS)



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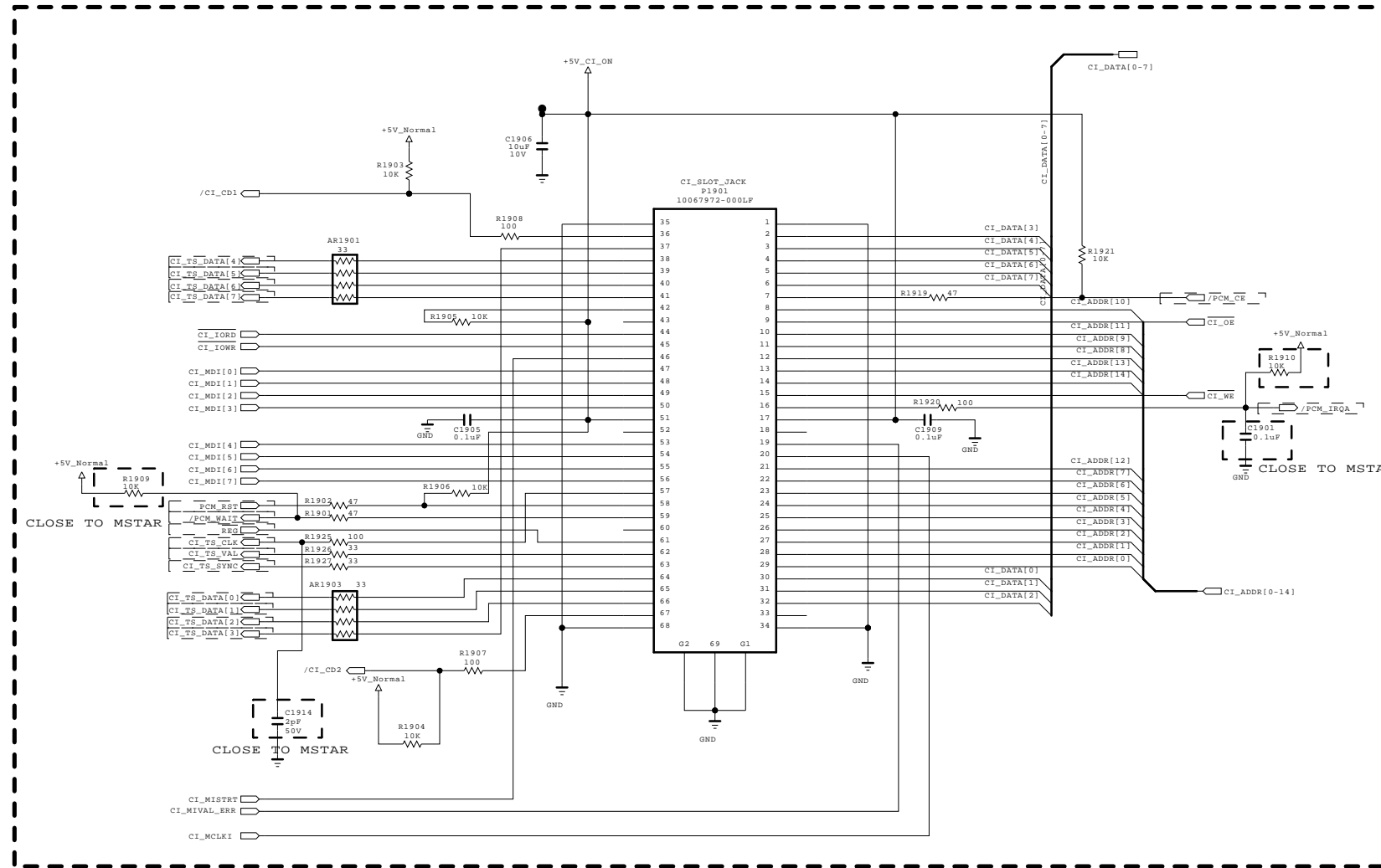
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LGElectronics



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|-------|------------|-------|------------|
| MODEL | NC4_S7LRM | DATE | 2012/06/20 |
| BLOCK | S_FLASH_OS | SHEET | 13 / |

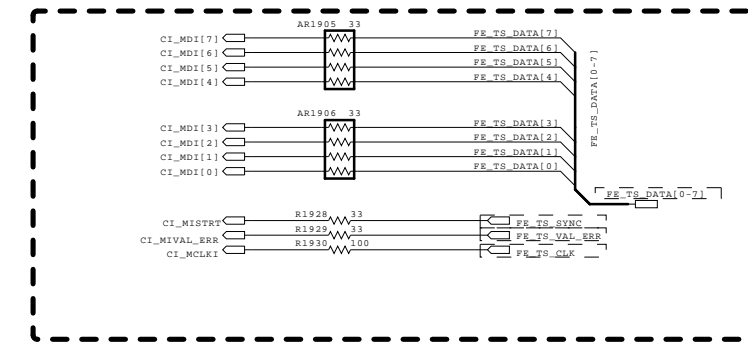
CI Region

CI SLOT

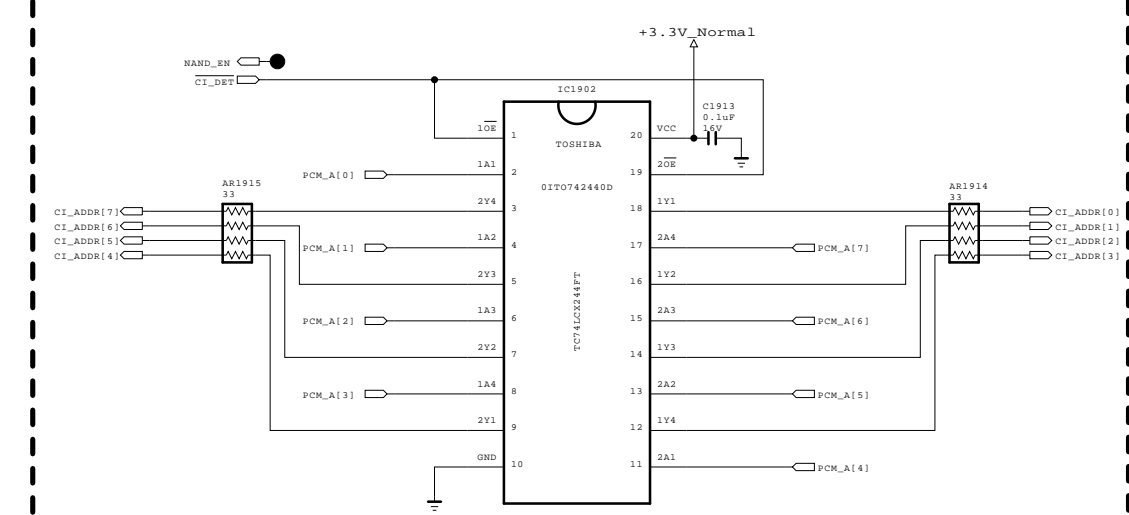


* Option name of this page : CI_SLOT
(because of Hong Kong)

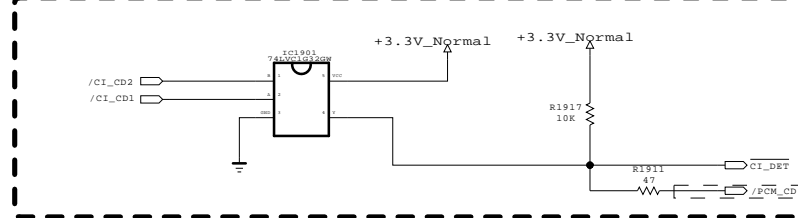
CI TS INPUT



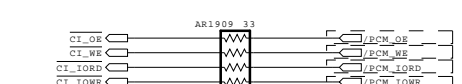
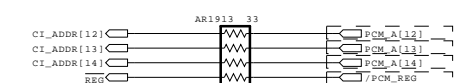
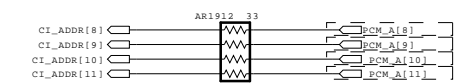
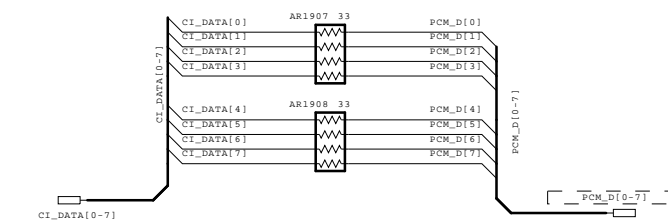
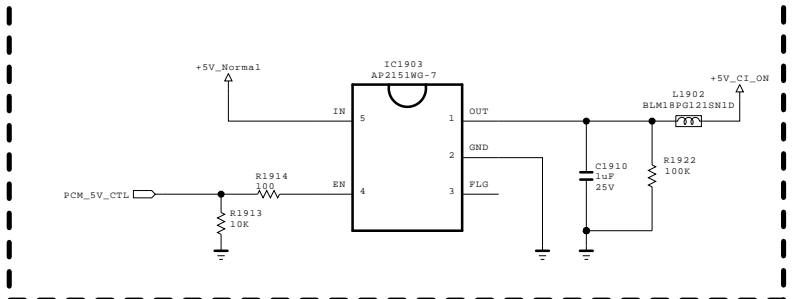
CI HOST I/F



CI DETECT



CI POWER ENABLE CONTROL



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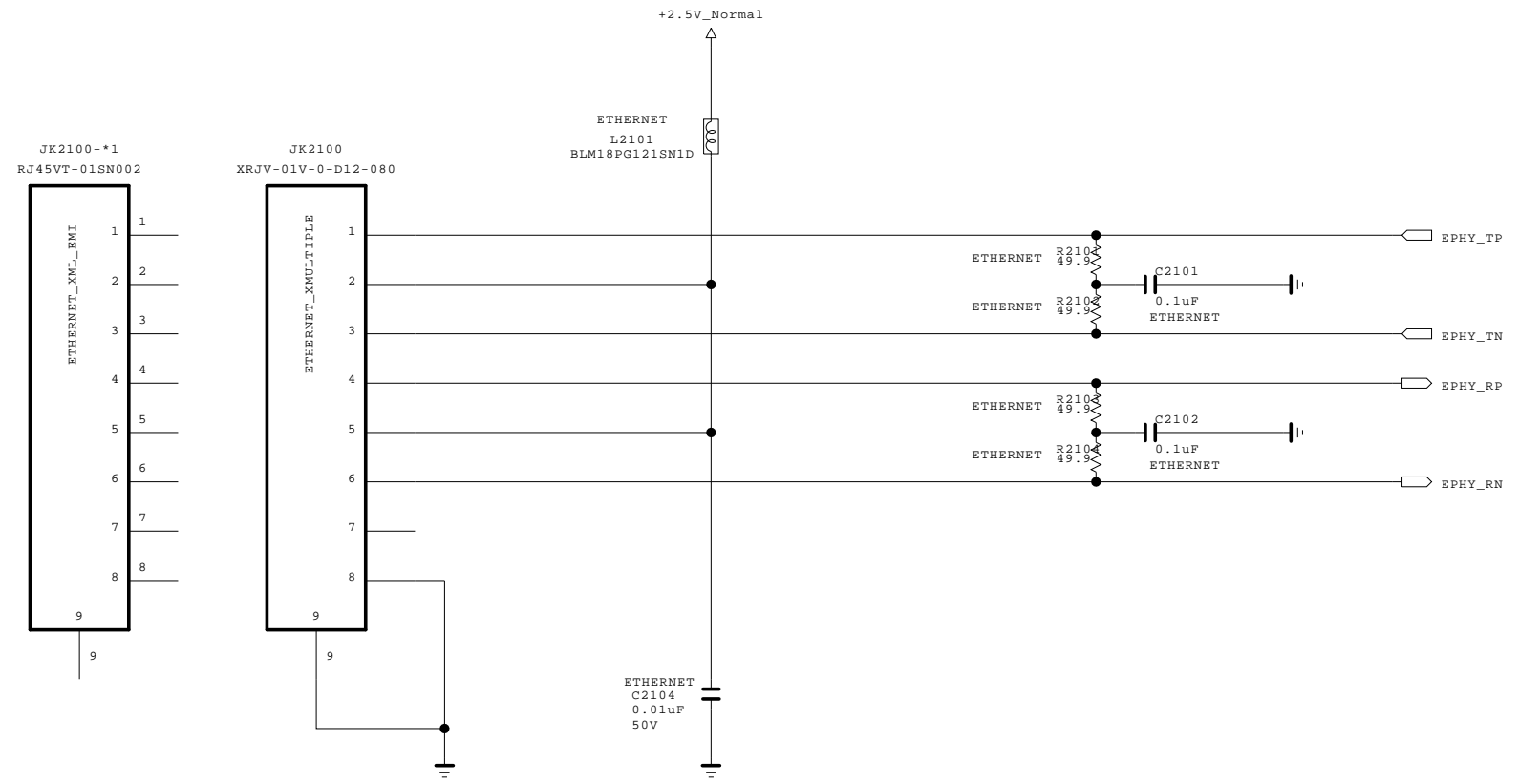
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| MODEL | NC4_S7LRM | DATE | 2012/06/19 |
| BLOCK | PCMCI | SHEET | 19 |

ETHERNET

* H/W option : ETHERNET



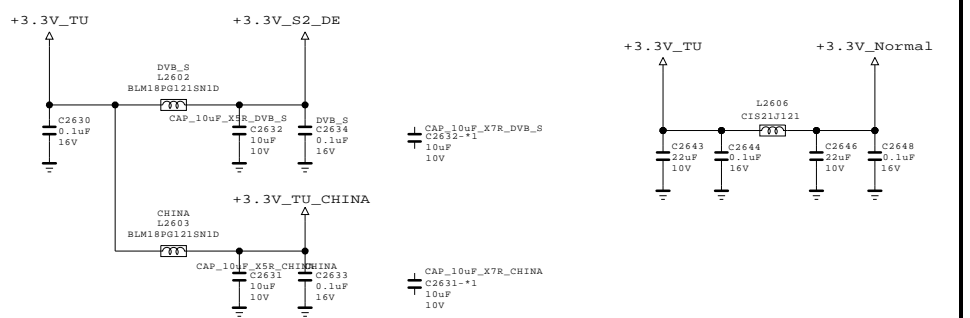
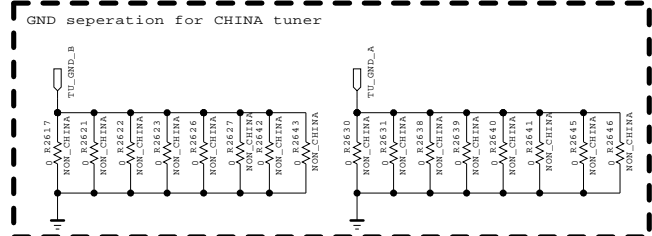
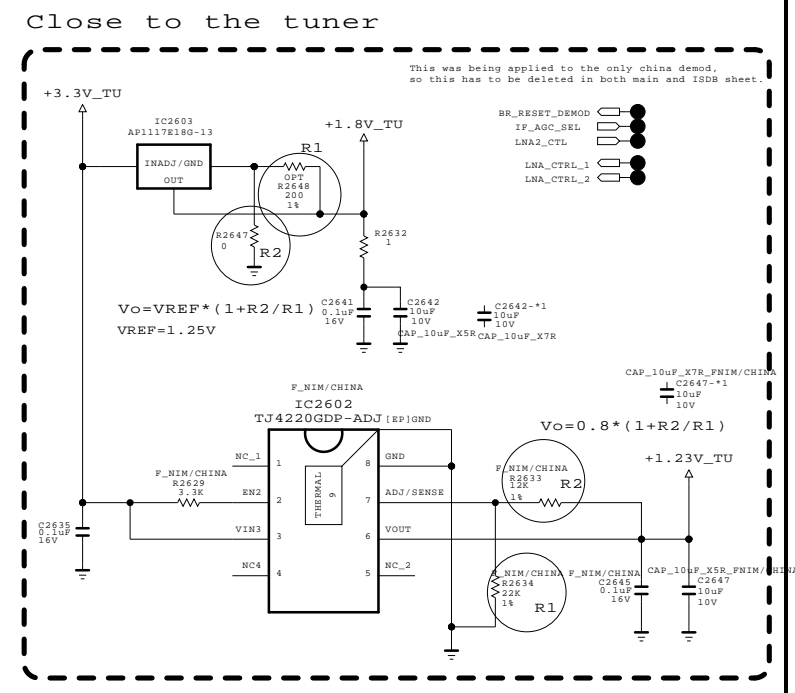
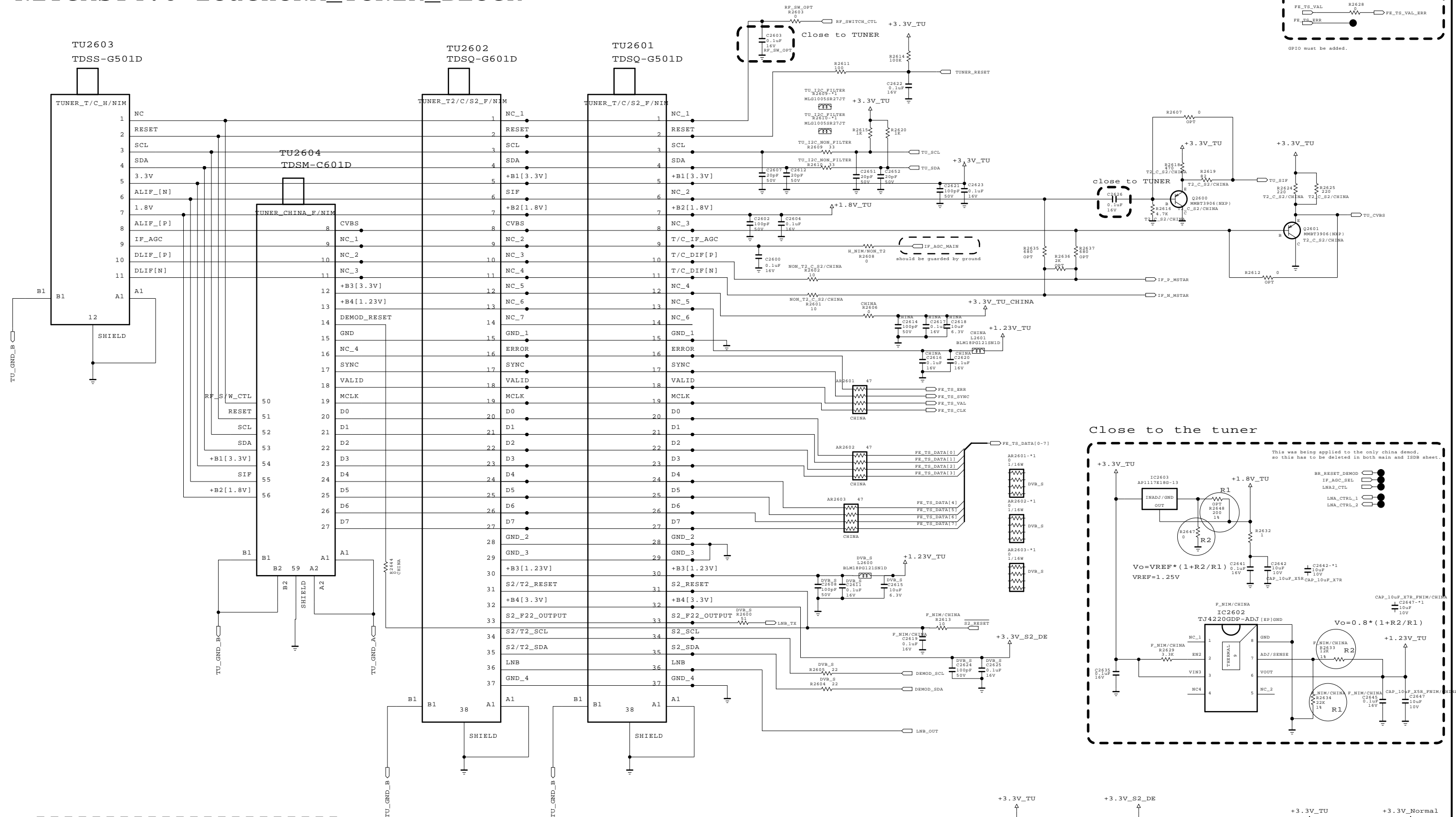
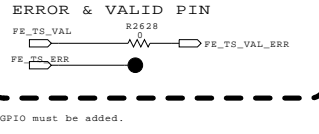
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| MODEL | NC4_S7LRM | DATE | 2012/06/21 |
| BLOCK | LAN | SHEET | 21 / |

NETCAST4.0 EU&CHINA_TUNER_BLOCK



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LGElectronics

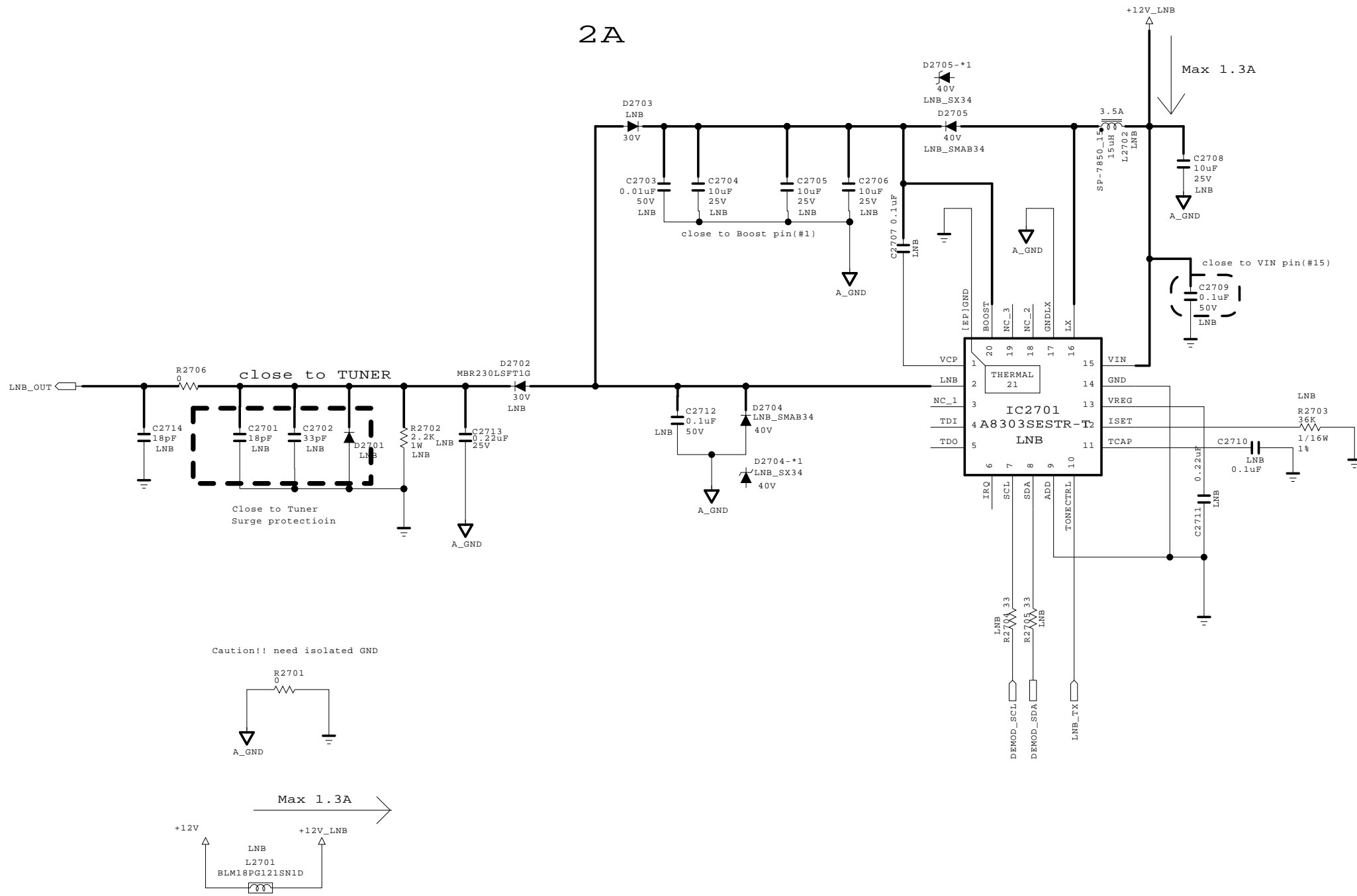




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| MODEL | NC4_S7LRM | DATE | 2012/06/19 |
| BLOCK | TUNER_EU | SHEET | 26 |

DVB-S2 LNB Part Allegro

(Option:LNB)

Input trace widths should be sized to conduct at least 3A
Output trace widths should be sized to conduct at least 2A

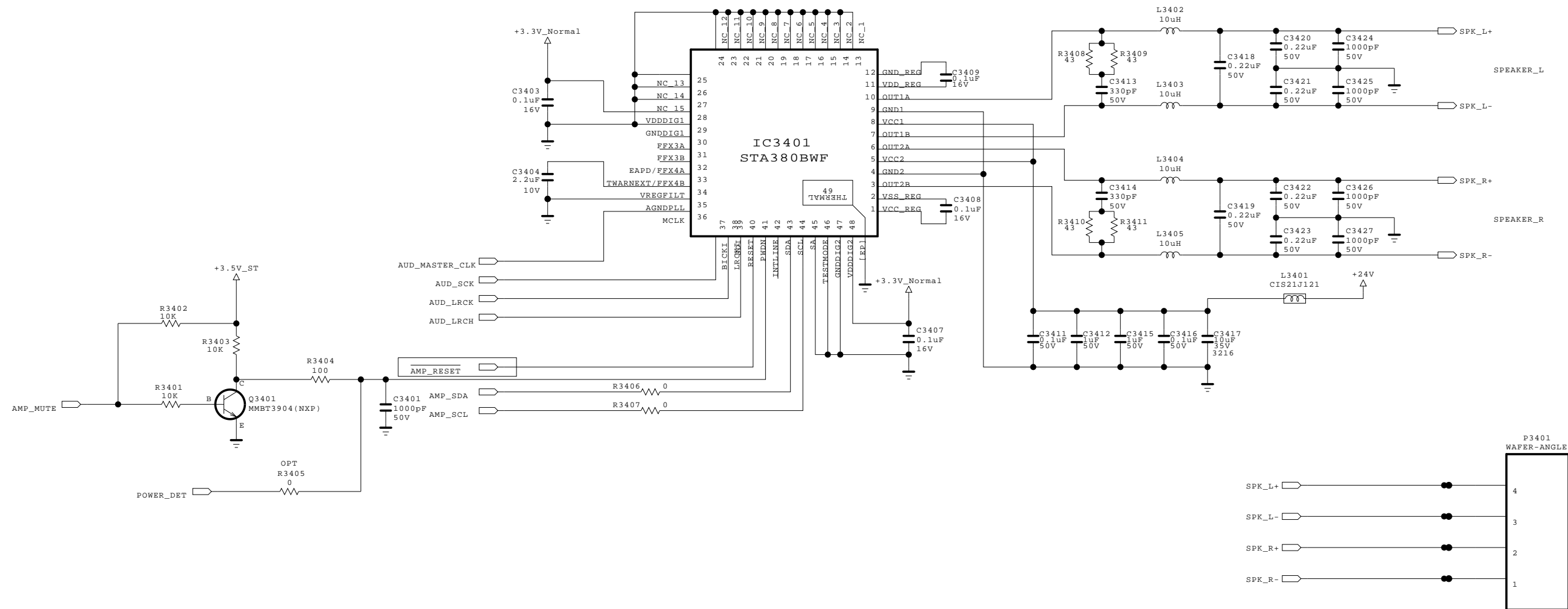




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| MODEL | NC4_S7LRM | DATE | 2012/06/19 |
| BLOCK | LNB | SHEET | 27 / |

AUDIO AMP (STA380BWEF)

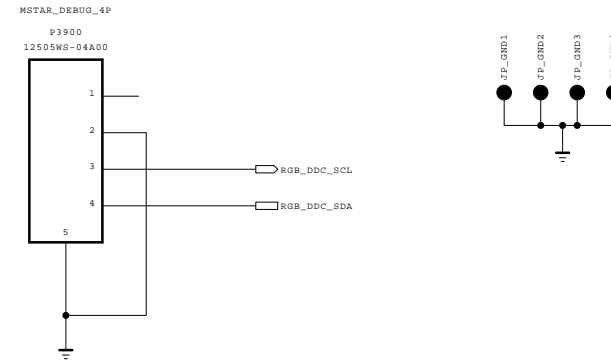


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| MODEL | NC4_S7LRM | DATE | 2012/08/29 |
| BLOCK | AMP_STA380BWEF | SHEET | 34 / |

MSTART DEBUG_4PIN



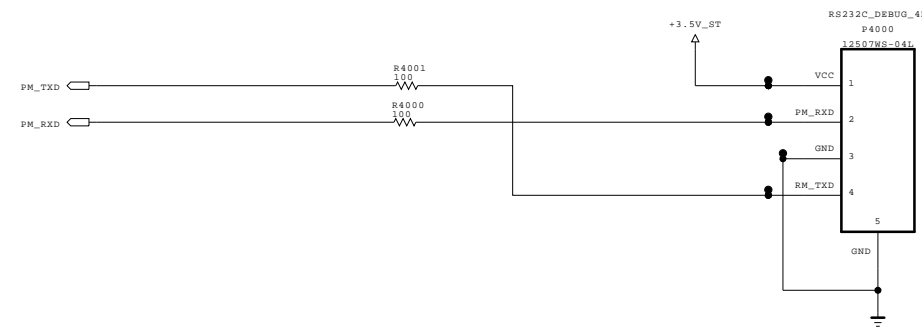
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| MODEL | NC4_S7LRM | DATE | 2012/06/20 |
| BLOCK | MSTAR_DEBUG_4PIN | SHEET | 39 / |

RS-232C



THE  SYMBOL MARK OF THIS SCHEMATIC DIAGRAM INCORPORATES SPECIAL FEATURES IMPORTANT FOR PROTECTION FROM X-RADIATION. FILRE AND ELECTRICAL SHOCK HAZARDS, WHEN SERVICING IF IS ESSENTIAL THAT ONLY MANUFACTURES SPECIFIED PARTS BE USED FOR THE CRITICAL COMPONENTS IN THE  SYMBOL MARK OF THE SCHEMATIC.

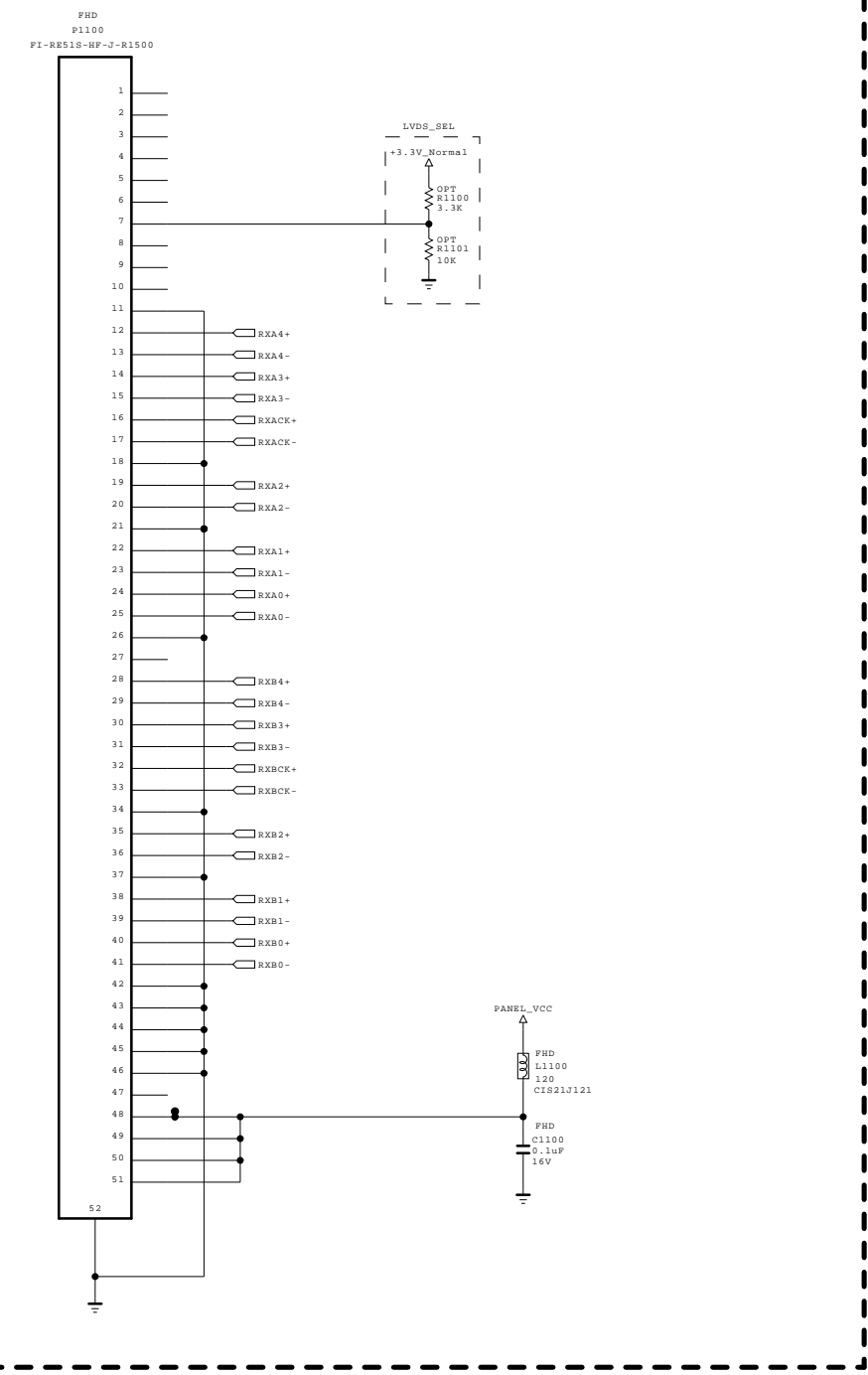
SECRET
LGElectronics



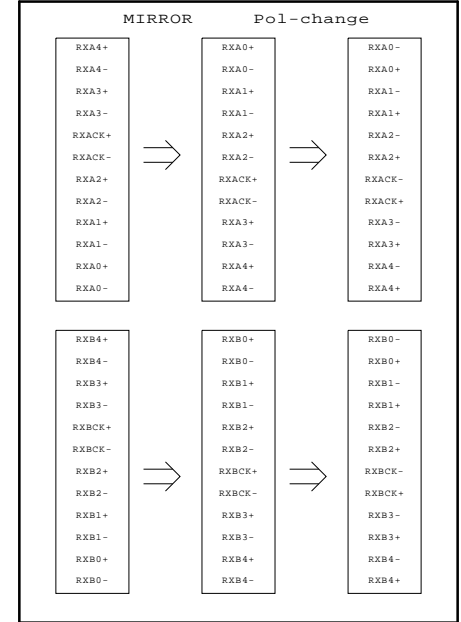
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|-------|--------------|-------|------------|
| MODEL | NC4_S7LRM | DATE | 2012/06/20 |
| BLOCK | RS232C_4P_OS | SHEET | 40 / |

LVDS (EU)

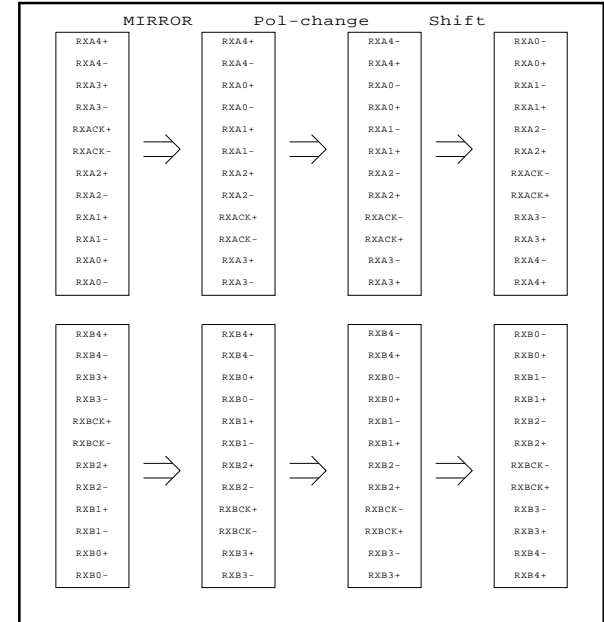
[51Pin LVDS Connector]
(For FHD 60Hz)



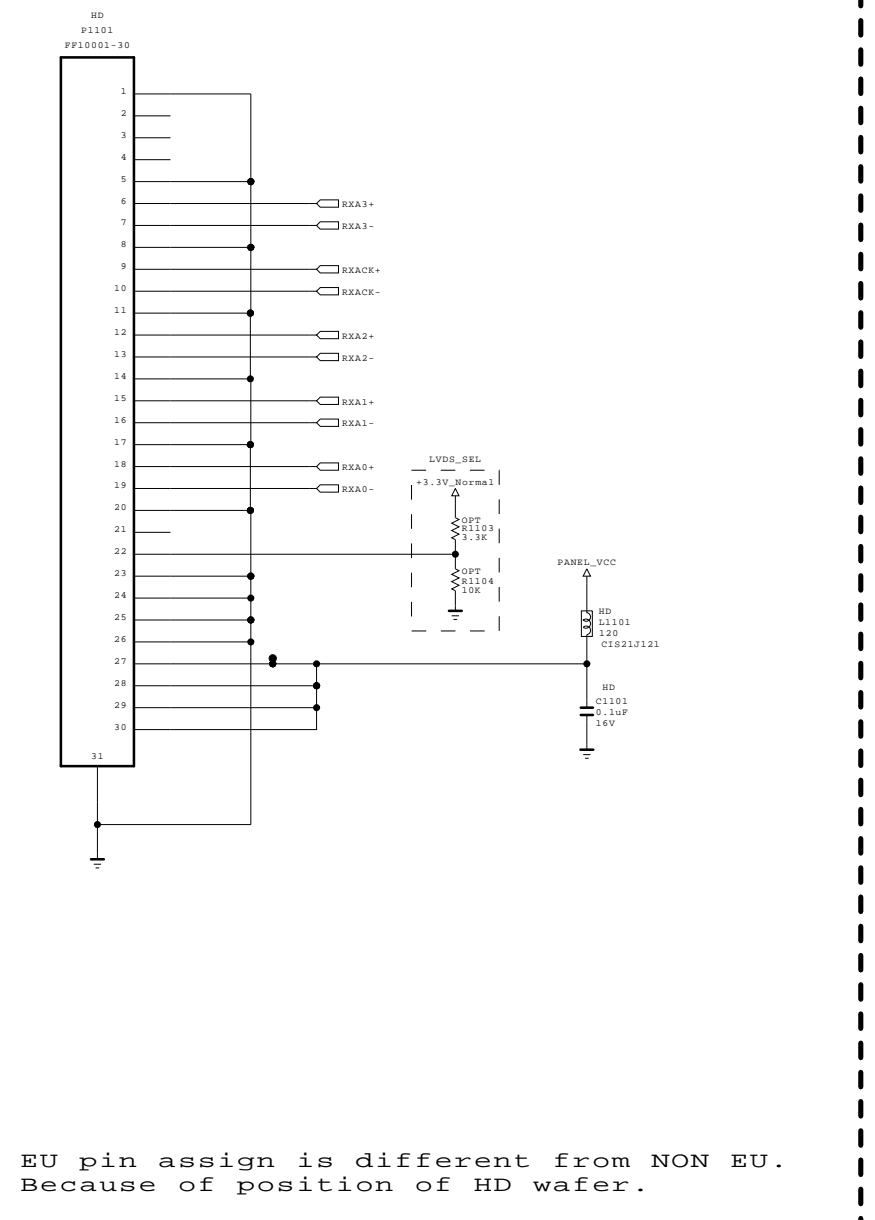
FOR FHD REVERSE(10bit)
Change in S7LR



FOR FHD REVERSE(8bit)
Change in S7LR



[30Pin LVDS Connector]
(For HD 60Hz_Normal)



EU pin assign is different from NON EU.
Because of position of HD wafer.

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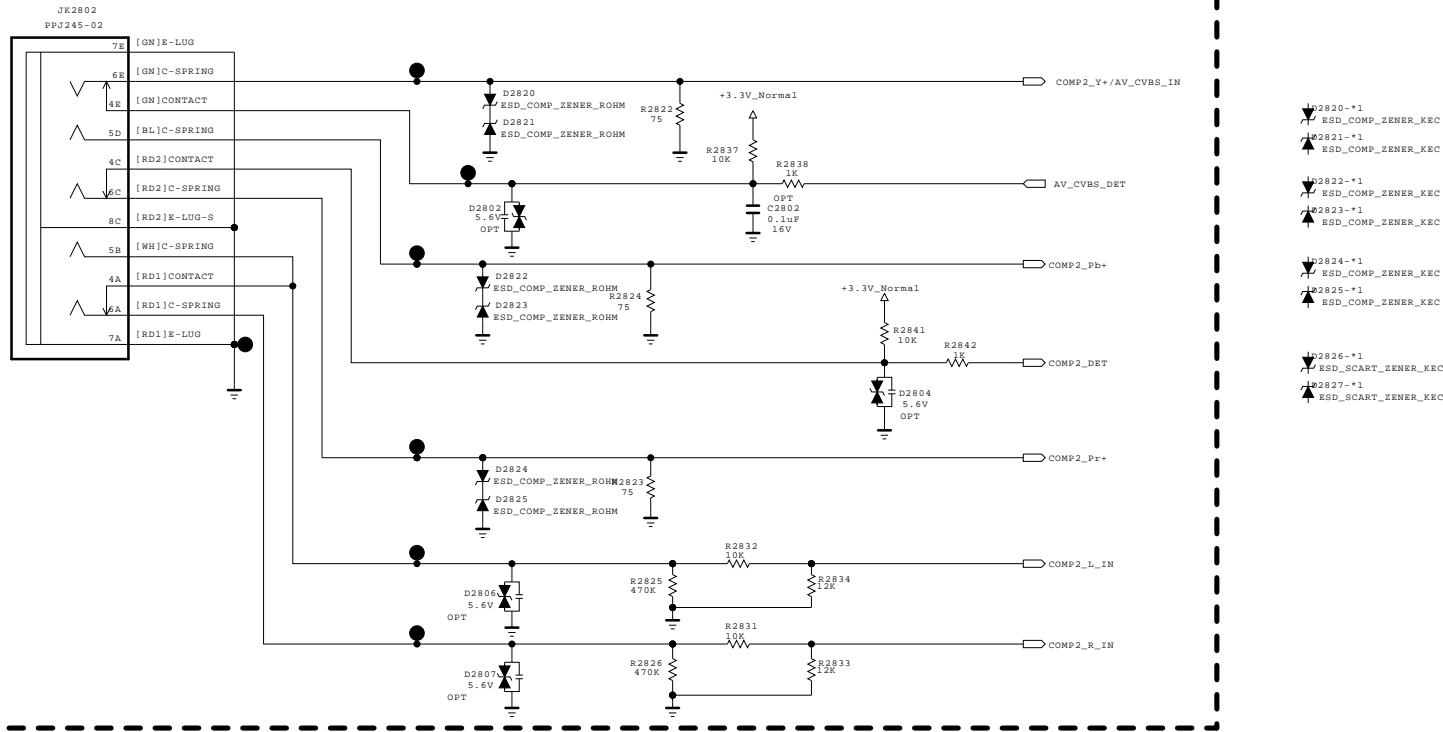
SECRET
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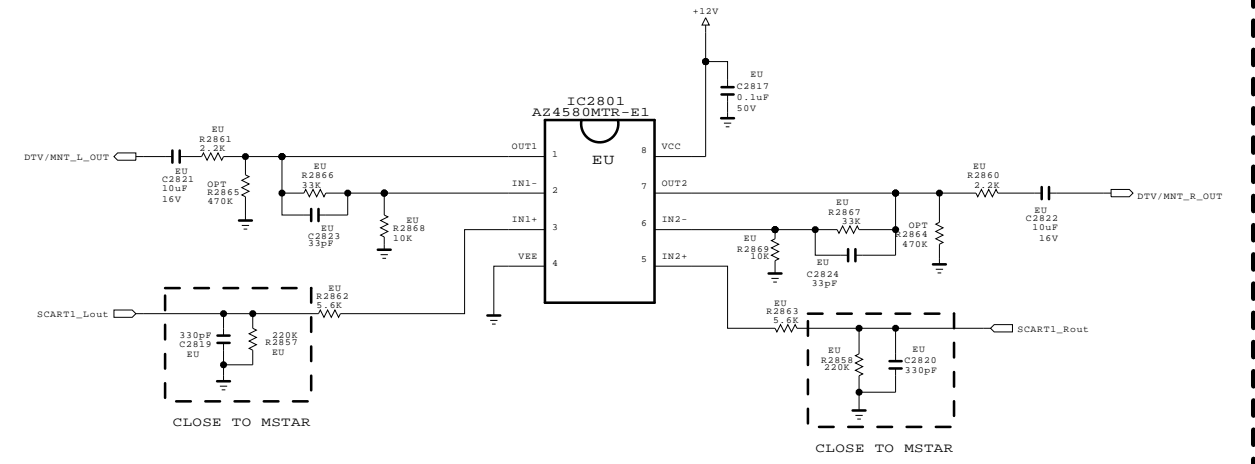
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| MODEL | NC4_S7LRM | DATE | 2012/06/22 |
| BLOCK | LVDS_EU | SHEET | 11 / |

SCART / COMPONENT&COMP SIT

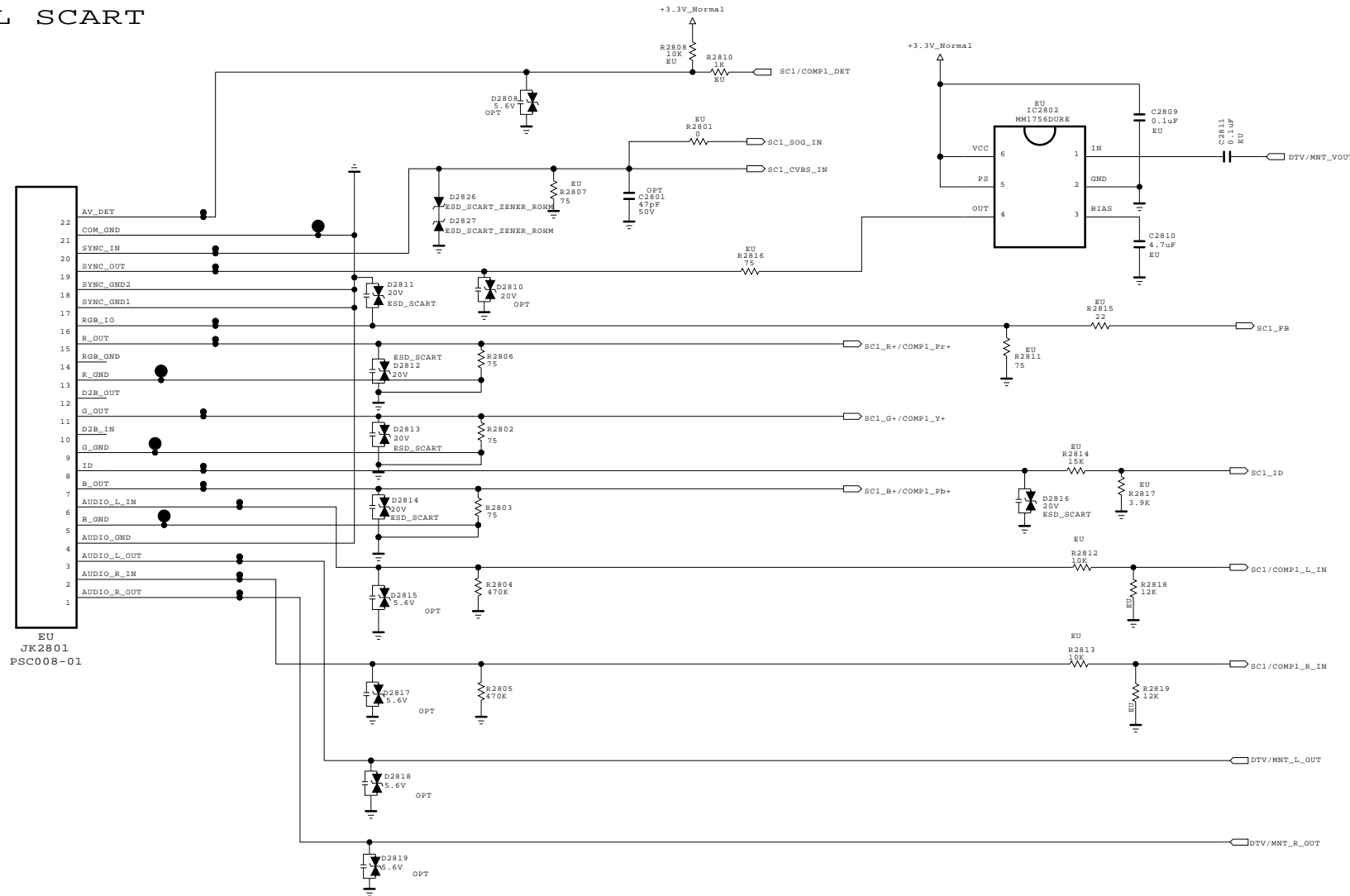
COMPONENT



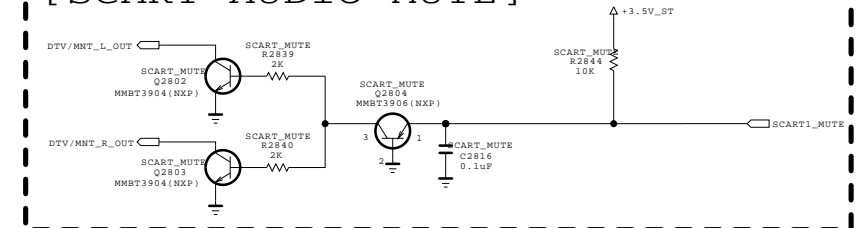
SCART AMP



FULL SCART



[SCART AUDIO MUTE]



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| MODEL | NC4_S7LRM | DATE | 2012/06/19 |
| BLOCK | REAR_JACK_EU | SHEET | 28 |